What is Claimed is:

1. A nonvolatile memory device including a write protected region, comprising:

a program command processor for outputting a program command signal by decoding an external signal;

a write protected region setting unit for storing a region address corresponding to an inputted address when the program command signal is activated, and for outputting a write protect signal when the program command signal is inactivated; and

a write controller for controlling a write operation not to be performed on a cell corresponding to the region address when the write protect signal is activated.

2. The device according to claim 1, wherein the program command signal is activated if an output enable signal toggles a predetermined number of times when a chip selection signal and a write enable signal are activated.

3. The device according to claim 2, wherein the program command signal is inactivated after the program command signal has been activated for the predetermined number of times.

4. The device according to claim 1, wherein the register comprises:

a first amplifier for amplifying and fixing a voltage at a node having a higher potential, of a first node and a second node, into a predetermined positive voltage in response to a first control signal;

a second amplifier for amplifying and fixing a voltage at a node having a lower potential, of the first node and the second node, into a ground voltage in response to a second control signal;

an input unit for providing a data signal to the first node and the second node in response to a third control signal; and

a storage unit for storing the signal provided to the first node and the second node in response to a fourth signal, where the stored signal is maintained when a power source is off,

wherein voltages of the first node and the second node are externally outputted.

5. The device according to claim 4, wherein the first amplifier comprises:

a first PMOS transistor having a gate to receive the

first control signal, and a source connected to a positive power source;

a second PMOS transistor having a gate connected to the first node, a source connected to a drain of the first PMOS transistor, and a drain connected to the second node; and

a third PMOS transistor having a gate connected to the second node, a source connected to the drain of the first PMOS transistor, and a drain connected to the first node.

6. The device according to claim 4, wherein the second amplifier comprises:

a first NMOS transistor having a gate connected to the first node, and a drain connected to the second node;

a second NMOS transistor having a gate connected to the second node, and a drain connected to the first node; and

a third NMOS transistor having a gate to receive the second control signal, a drain connected to a source of the first NMOS transistor and a source of the second transistor, and a source connected to a ground.

7. The device according to claim 4, wherein the

input unit comprises:

a first NMOS transistor having a gate to receive the third control signal, a source to receive a first data signal, and a drain connected to the first node; and

a second NMOS transistor having a gate to receive the third control signal, a source to receive a second data signal, and a drain connected to the second node.

8. The device according to claim 4, wherein the storage unit comprises:

a first ferroelectric capacitor connected between the fourth control signal and the first node;

a second ferroelectric capacitor connected between the fourth control signal and the second node;

a third ferroelectric capacitor connected between the first node and a ground; and

a fourth ferroelectric capacitor connected between the second node and a ground.

9. The device according to claim 1, wherein the write protect region setting unit comprises:

a register array for storing the region address; and

a comparator for comparing a region address corresponding to the inputted address with an address

stored in the register array, and outputting the write protect signal.

10. The device according to claim 9, wherein the write protected region setting unit further comprises a second register array having the same number of the register array,

wherein the comparator compares the rest region address bits with the address bits stored in the register array except region address bits corresponding to activated bits stored in the second register array while an external control signal is activated, and outputs the write protect signal.

11. The device according to claim 9, wherein the write protected region setting unit further comprises a master register, and the write protect signal is not activated when a signal stored in the master register is not activated.

12. The device according to claim 10, wherein the write protected region setting unit further comprises a master register, and the write protect signal is not activated when a signal stored in the master register is

not activated.

13. The device according to claim 1, wherein the write controller controls a write mode not to be performed on a memory region corresponding to the region address when the write protect signal or the external control signal is activated.

14. A nonvolatile memory device including a write protected region, comprising:

a first register array including a pluarlity of registers where a region address is stored;

a second register array including a plurality of registers corresponding to the plurality of registers;

a master register for controlling activation; and

a comparator for comparing a region address stored in the first register array with an externally inputted region address except those address bits corresponding to activated registers of the second register array, in response to an output value of the master register, and then outputting a comparison result.

15. A nonvolatile memory device including a write protected region, comprising:

an internal protection signal controller for receiving an externally inputted address and an address of a predetermined protected region, and outputting an internal protection signal;

an external protection signal controller for outputting an external protection signal in response to an external control signal;

a write protect controller for receiving the internal protection signal and the external protection signal, and outputting a write protect signal; and

a write controller for controlling read/write operations of the memory device in response to the write protect signal and a write enable signal.